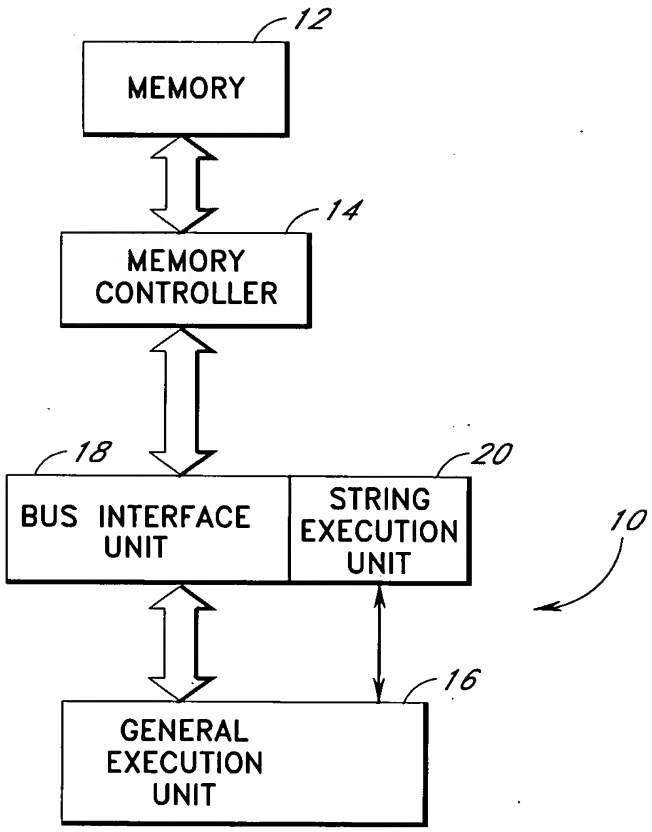
12
MEMORY
14
MEMORY CONTROLLER
18
20
BUS INTERFACE UNIT
STRING EXECUTION UNIT
10
16
GENERAL EXECUTION UNIT

FIG. 1

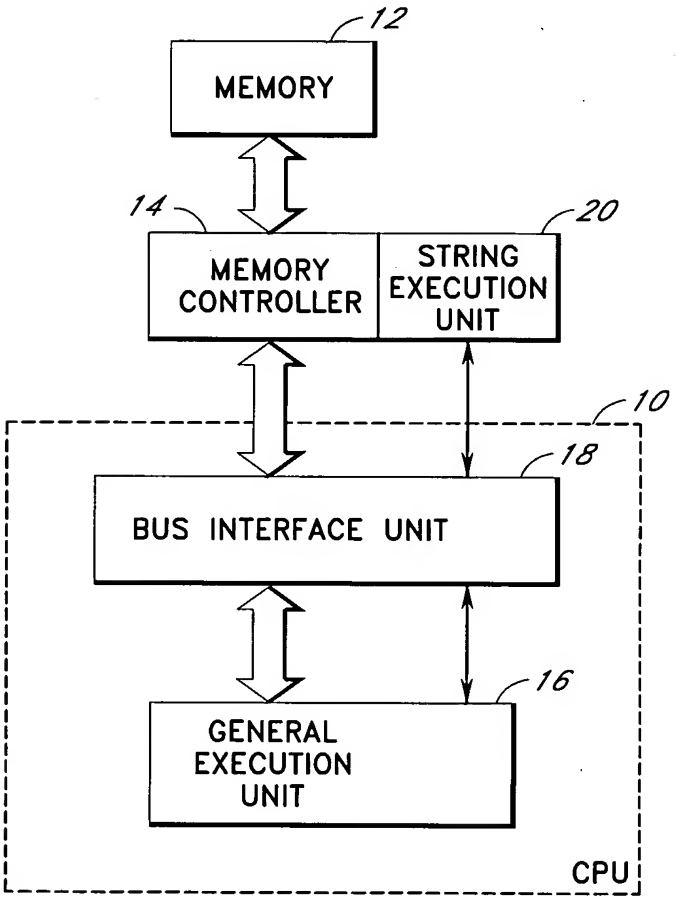
12
MEMORY
14
20
MEMORY CONTROLLER
STRING EXECUTION UNIT
10
18
BUS INTERFACE UNIT
16
GENERAL EXECUTION UNIT
CPU

FIG. 2

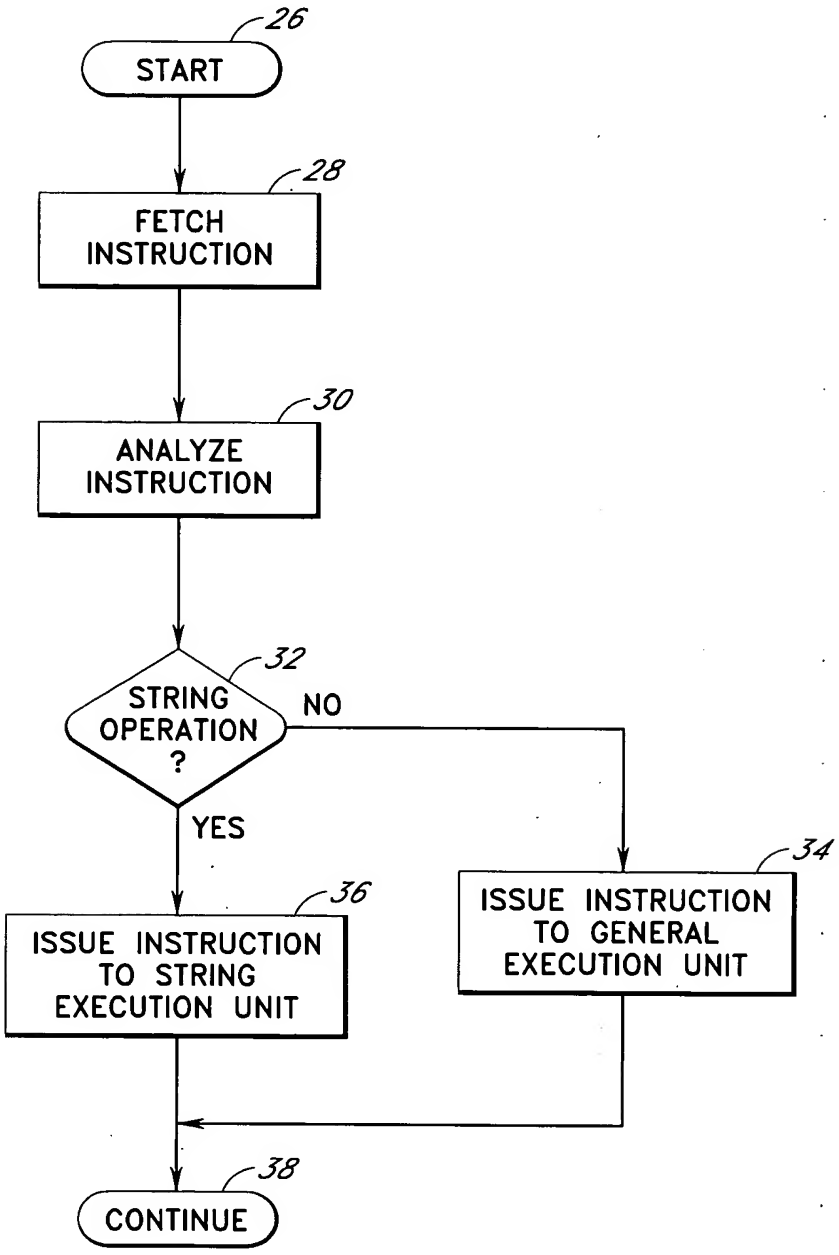
26
START
28
FETCH INSTRUCTION
30
ANALYZE INSTRUCTION
32
STRING OPERATION ?
NO
YES
34
ISSUE INSTRUCTION TO GENERAL EXECUTION UNIT
36
ISSUE INSTRUCTION TO STRING EXECUTION UNIT
38
CONTINUE

FIG. 3

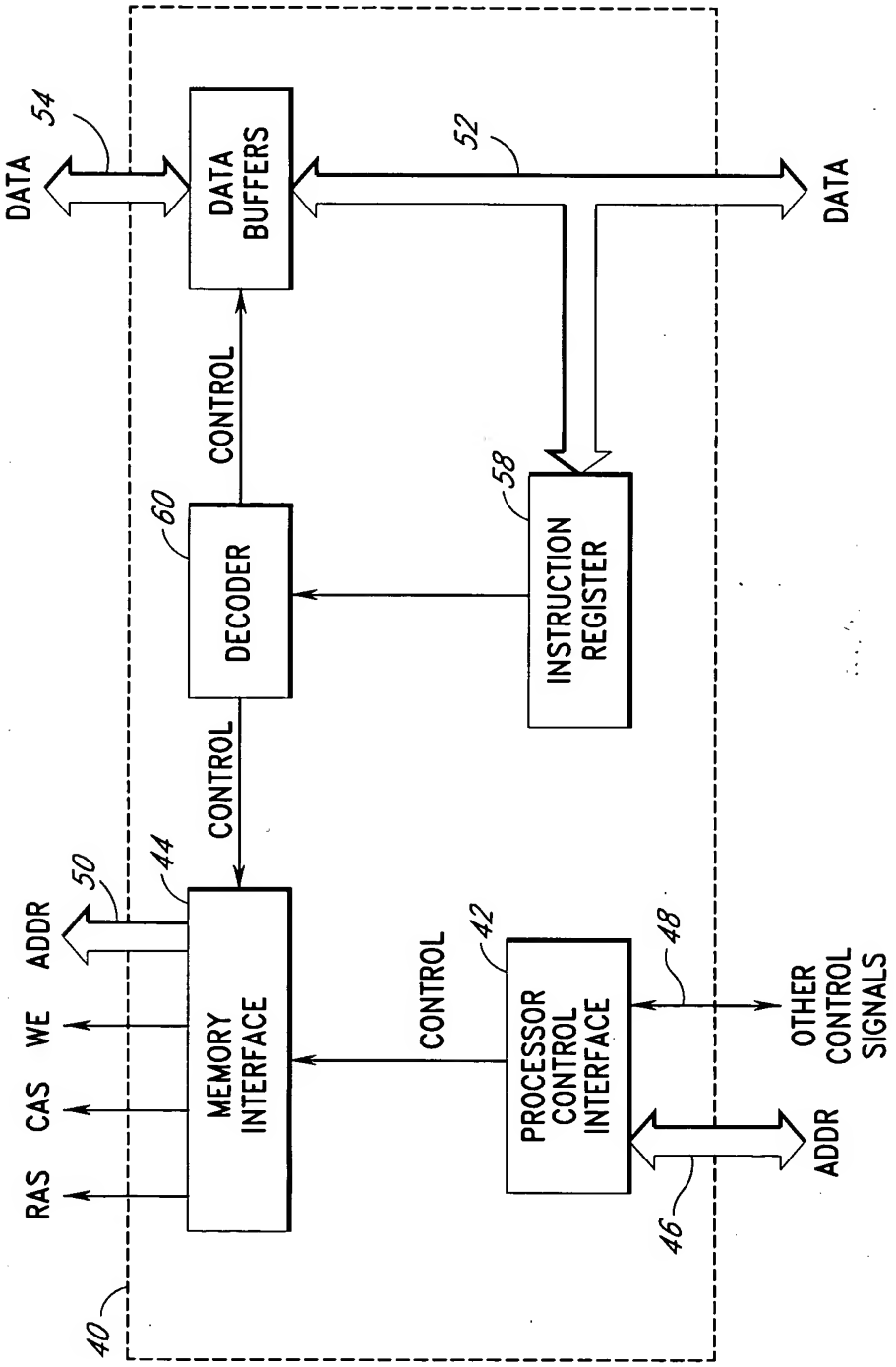
DATA
54
DATA BUFFERS
52
DATA
CONTROL
60
DECODER
58
INSTRUCTION REGISTER
CONTROL
44
50
ADDR
WE
CAS
RAS
MEMORY INTERFACE
CONTROL
42
PROCESSOR CONTROL INTERFACE
48
OTHER CONTROL SIGNALS
ADDR
46
40

FIG. 4

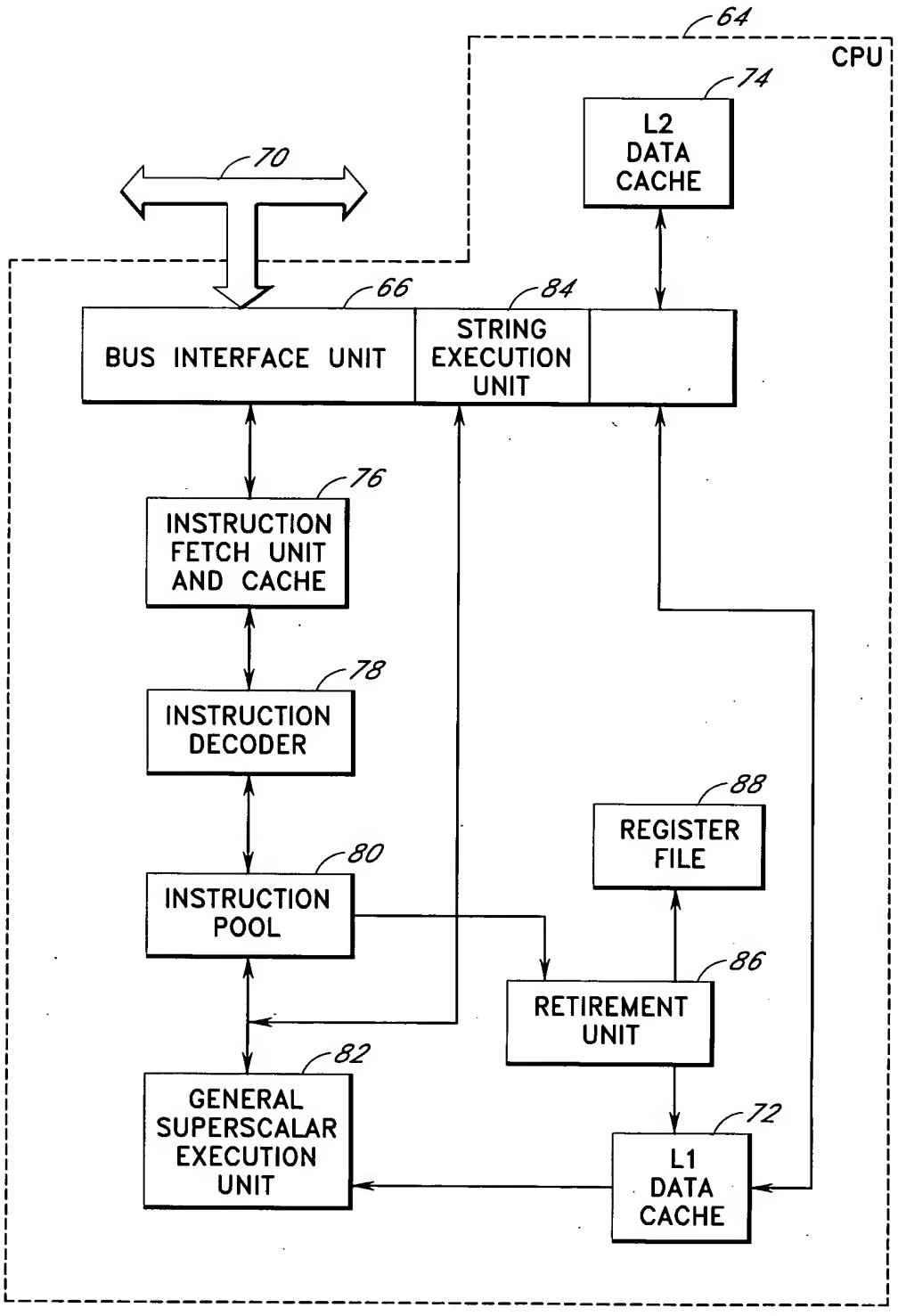
64
CPU
74
L2
DATA
CACHE
70
66
84
BUS INTERFACE UNIT
STRING
EXECUTION
UNIT
76
INSTRUCTION
FETCH UNIT
AND CACHE
78
INSTRUCTION
DECODER
88
REGISTER
FILE
80
INSTRUCTION
POOL
86
RETIREMENT
UNIT
82
GENERAL
SUPERSCALAR
EXECUTION
UNIT
72
L1
DATA
CACHE

FIG. 5

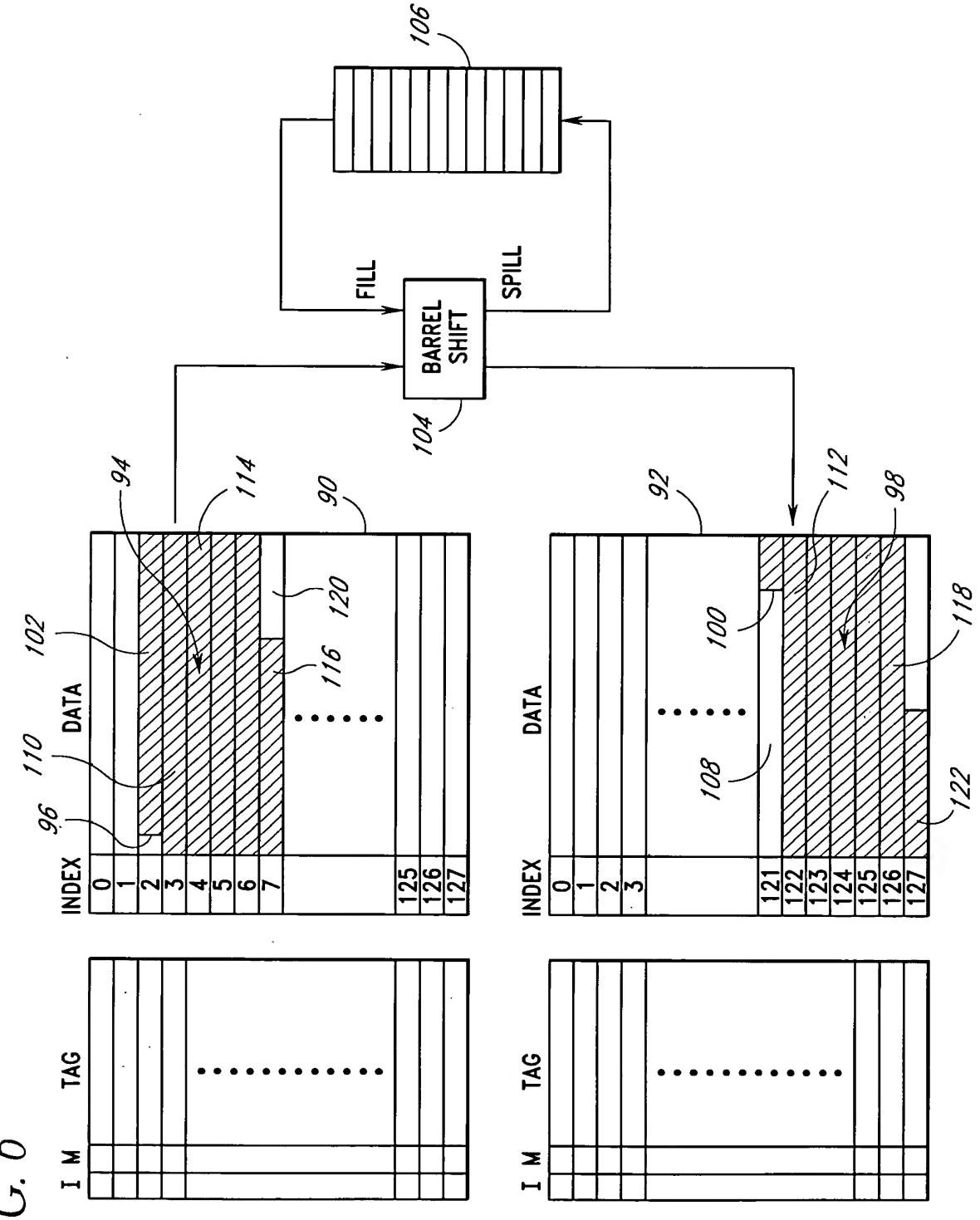
106
FILL
SPILL
BARREL SHIFT
104
94
114
90
92
112
98
102
120
116
100
118
110
DATA
108
96
122
INDEX
0
1
2
3
4
5
6
7
125
126
127
121
122
123
124
TAG
I M

FIG. 6

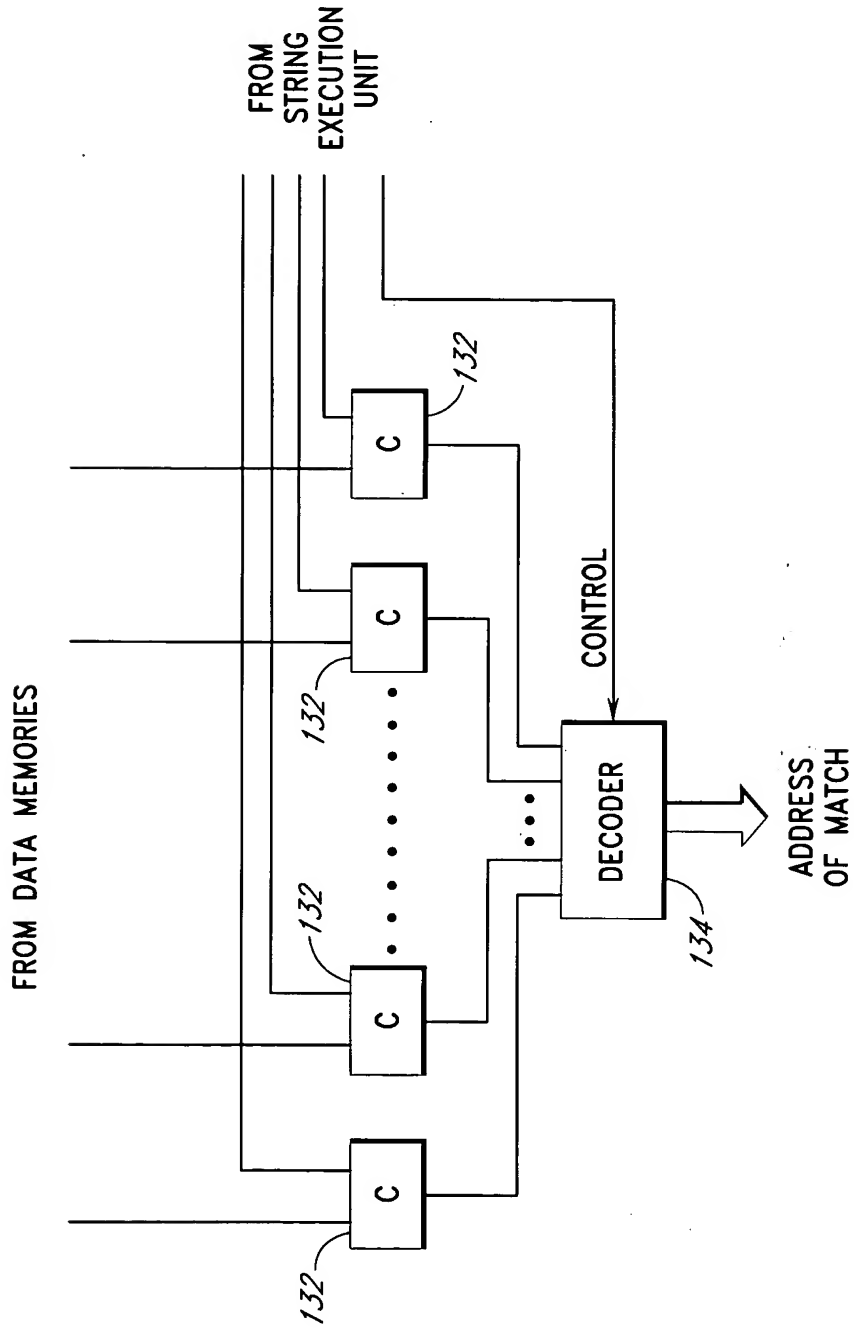
FROM STRING EXECUTION UNIT
FROM DATA MEMORIES
CONTROL
C
132
DECODER
134
ADDRESS OF MATCH

FIG. 7